REMARKS

In the November 3, 2004 Office Action, the Examiner:

- Rejected claim 12 under 35 U.S.C. 112, second paragraph, as being indefinite;
- Rejected claims 1-13 under 35 U.S.C. 103(a) as unpatentable over King et al. ("*King*", U.S. Pat. No. 5,812,572) in view of Stephenson ("*Stephenson*", U.S. App. No. 2002/0027688) and Swartz ("*Swartz*", U.S. Pat. No. 6,021,947);
- Provisionally rejected claims 1-13 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over various combinations of *King*, *Stephenson, Swartz,* and copending application nos. 09/777,917, or 10,713,685.

Applicants have revised claims 1-12. The pending claims remain claims 1-13.

The revisions to claims 1 and 4 with respect to disabling operation of "at least part of" the transceiver are supported by at least paragraph 0064 of the specification. The revision to claim 1 with respect to "enabling the host to read from the at least one predefined location in the memory" is supported by at least paragraph 0047 of the specification.

Claim Rejections - 35 U.S.C. § 112

Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner states that insufficient antecedent basis exists in claim 12 for "the predefined memory mapped locations" in line 10 of the claim and "the memory" in line 14 of the claim. Claim 12 has been amended to correct typographical errors. Accordingly, it is respectfully submitted that the Examiner's 35 U.S.C. 112 rejections have been addressed.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 1-13 under 35 U.S.C. 103(a) as unpatentable over *King* in view of *Stephenson* and *Swartz*. To establish a prima facie case of obviousness, three basic criteria must be met, namely:

1) There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;
2) There must be a reasonable expectation of success; and
3) The prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure.[1]

This set of rejected claims contains four independent claims, namely claims 1, 4, 8 and 12. Both claims 1 and 4 contain the limitation of "an interface configured to enable a host to read from and write to host specified locations within the memory". Claim 8 includes the limitation of "an interface for allowing a host to read from and write to host specified locations within the memory", and claim 12 requires "in accordance with instructions received from a host device, enabling the host device to read from and write to host specified locations within a controller of the optoelectronic transceiver". In other words, the host device can read from specific locations within the memory (or controller) of the optoelectronic transceiver and does not have to read an entire diagnostics file from the memory (or controller) in order to examine the state of the transceiver. This has many advantages, including speed of data access, reduction in bandwidth used between the optoelectronic transceiver and the host device, improved efficiency, reduced load and wear on the memory, *etc.*

With regard to this limitation, the Examiner states that *King* discloses "an interface 26 configured to enable a host (such as computer 90 in Figure 3) to read from and write to host-specified locations within the memory (column 10, lines 10-18; column 16, lines 58-63)", (emphasis added). However, the host computer 90 disclosed by *King* is only able to interrogate or communicate with the microcontroller 50 and not with the PROM, RAM or EEPROM.[2] Accordingly, there is no teaching in *King* that the host computer can specify memory locations, or any other memory-mapped locations within the laser transmitter module. In other words, *King* does not disclose, teach or suggest a host device that can read from and write to host specified locations within a memory (or controller). Furthermore, neither *Stephenson* nor *Swartz* disclose, teach or suggest a memory interface for allowing a

---

[1] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

[2] *See King* col. 16, lines 58-67, and Figure 1.

host to read from host specified locations within the memory. For this reason alone, independent claims 1, 4, 8 and 12, and their dependant claims 2-3, 5-7, 9-11 and 13, cannot be unpatentable over *King* in view of *Stephenson* and *Swartz*.

Furthermore, regarding claim 9, the Examiner states that *King* discloses that the adjustment value corresponds to a deviation from a configured operating condition of the optoelectronic transceiver, since the control signals disclosed by King et al. are adjusted based on deviations in operating conditions (such as temperature or power; column 16, lines 26-31). The section of *King* relied on by the Examiner states:

> A possible laser control algorithm would proceed as follows: step 236, measure current operating conditions (i.e. temperature and/or power supply), and compute index into table or solve polynomial equations based on operating conditions; step 238, update tracking error adjust DAC 44, and update modulation current control DAC 24; step 240,

In other words, *King* measures the operating conditions and computes an index from the operating conditions. *King* does not, however, teach an adjustment value that is stored in the memory by the host, where the adjustment value is used to adjust one or more control signals and corresponds to a deviation from a configured operating condition of the optoelectronic transceiver. In fact, there is no mention in *King* whatsoever of a deviation from a configured operating condition.

Finally, independent claims 1, 4 and 8 now include the limitation of storing a digital value in at least one predefined location in the memory, while independent claim 12 requires generating control signals in accordance with one or more values stored in predefined memory mapped locations within the controller. In related applications, these limitations were indicated to be allowable subject matter. Accordingly, for this reason alone, independent claims 1, 4, 8 and 12, and their dependent claims, are now in condition for allowance.

Double Patenting

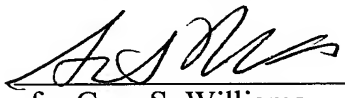
The Examiner has provisionally rejected numerous claims under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims of copending applications 09/777,917 and 10/713,685. Pursuant to 37 CFR 1.321(c), Applicants hereby submit a terminal disclaimer to overcome these provisional rejections.

CONCLUSION

In light of the amendments to the claims, the arguments presented above, and the terminal disclaimer, Applicants respectfully request that the Examiner reconsider this application with a view towards allowance. The Examiner is encouraged to call the undersigned attorney at (650) 843-4000 should any issues remain unresolved.

Furthermore, if there are any fees or credits due in connection with the filing of this Response, including any fees required for an Extension of Time under 37 C.F.R. Section 1.136, authorization is given to charge any necessary fees to our Deposit Account No. 50-0310 (order No. 060900-0197-US). A copy of this sheet is enclosed for such purpose.

Respectfully submitted,

Date: January 31, 2005  31,066

for Gary S. Williams
MORGAN, LEWIS & BOCKIUS LLP
2 Palo Alto Square
3000 El Camino Real, Suite 700
Palo Alto, California 94306
(650) 843-4000